



# Bridgeless Discontinuous Conduction Mode SEPIC Power Factor Correction Rectifier

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**(Abstract)** This paper deals with modelling and simulation of Single phase AC-DC Bridgeless Discontinuous Conduction Mode (DCM) with Single Ended Primary Inductance Converter (SEPIC) for Power Factor Correction (PFC) rectifier. The topology is improved by the absence of an input diode bridge and the presence of only two semiconductor switches in the current flowing path during each switching cycle which results in lesser conduction losses and improved thermal management compared to the conventional SEPIC converters. By implementing the improved topology in DCM it ensures almost unity power factor in a simple and effective manner. The DCM operation gives additional advantages such as zero-current turn-on in the power switches, zero-current turn-off in the output diode and reduces the complexity of the control circuitry. Performance comparisons between the improved and conventional SEPIC PFC rectifier are carried out using Pspice software and results are presented.

**Keywords:** Discontinuous Conduction Mode (DCM), Single Ended Primary Inductance Converter (SEPIC), Power Factor Correction (PFC).

## 1. INTRODUCTION

SEPIC is a DC/DC converter topology that provides a positive regulated output voltage from an input voltage that varies from above to below the output voltage. This type of conversion is handy when the designer uses voltages from an unregulated input power supply. Hence this is very much preferred in applications such as battery chargers, power electronic circuits, home appliances, aircraft due to its less electromagnetic interference, inherent inrush current, reduced noise disturbances and less switching losses.

The SEPIC topology is difficult to understand and requires two inductors, making the power-supply quite large. Recently, several inductor manufacturers began selling off-the-self coupled inductors in a single package at a cost only slightly higher than that of the comparable single inductor. The coupled inductor not only provides a smaller footprint but also, to get the same inductor ripple current, requires only half the inductance required for a SEPIC with two separate inductors.

Most of the presented bridgeless topologies so far [1]–[9] implement a boost-type circuit configuration (also referred to as dual-boost PFC rectifiers) because of its low cost and its high performance in terms of efficiency, power factor, and simplicity. These features have led power supply companies to start looking for bridgeless PFC circuit topologies. In [7], a systematic review of the bridgeless PFC boost rectifier implementations that have received the most attention is presented along with their performance comparison with the conventional PFC boost rectifier. The bridgeless boost rectifier has the same major practical drawbacks as the

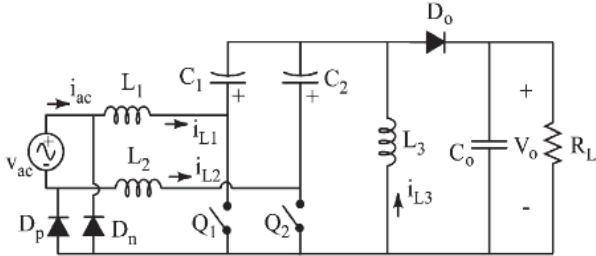
conventional boost converter, such that the dc output voltage is always higher than the peak input voltage, input–output isolation cannot easily be implemented, the start up inrush current is high, and there is a lack of current limiting during overload conditions. Moreover, it is well known that the boost converter operating in discontinuous current mode (DCM) can offer a number of advantages such as inherent PFC function, very simple control, soft turn-on of the main switch, and reduced diode reversed-recovery losses. However, the DCM operation requires a high-quality boost inductor since it must switch extremely high peak ripple currents and voltages. As a result, a more robust input filter must be employed to suppress the high-frequency components of the pulsating input current, which increases the overall weight and cost of the rectifier.

The operation of SEPIC is similar to the bridgeless buck-boost PFC converter which has only three conduction semiconductors at every moment[1]. Comparing with the cascade buck-boost CBB-PFC converter, the efficiency is increased. Power factor is more than 0.98, and total harmonic distortion (THD) is less than one.

The main features of the presented converter include high efficiency, low voltage stress on the semiconductor devices, and simplicity of design. These advantages are desirable features for high-power and high-voltage applications. The modelling and simulation result of Bridgeless Discontinuous Conduction Mode SEPIC Power Factor Correction rectifier is presented.

## 2. BRIDGELESS SEPIC PFC RECTIFIER

The bridgeless PFC circuits based on SEPIC with low conduction losses, is shown in Fig 1. Unlike the boost converter, the SEPIC converters offer several advantages in PFC applications, such as easy implementation of transformer isolation, inherent inrush current limitation during start-up and overload conditions, lower input current ripple, and less electromagnetic interference (EMI) associated with the DCM topology.



**Fig 1 : Bridgeless SEPIC PFC rectifier**

The topologies in Figure 1 are formed by connecting two DC–DC SEPIC Converter one for each half-line period of the input voltage. The operational circuits during positive and negative half-line period for the proposed bridgeless SEPIC rectifier of Fig.1 is shown respectively. Note that, by referring to Fig.1 there are one or two semiconductors in the current flowing path. Each of the rectifier utilizes two power switches ( $Q_1$  and  $Q_2$ ), two low-recovery diodes ( $D_p$  and  $D_n$ ), and a fast diode ( $D_o$ ). However, the two power switches can be driven by the same control signal, which significantly simplifies the control circuitry. Moreover, the structure of the proposed topologies utilizes one additional inductor compared to the conventional topologies, which are often described as a disadvantage in terms of size and cost.

However, better thermal performance can be achieved with the two inductors compared to a single inductor. This is because each power switch is operating during half-line period. On the other hand, the components voltage stresses are equal to their counterparts in the conventional SEPIC converter.

### 3 . PRINCIPLE OF OPERATION OF THE BRIDGELESS RECTIFIER

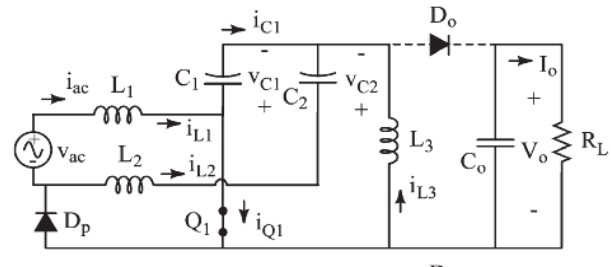
The bridgeless rectifier shown in Figure 1 is constructed by connecting two DC–DC converters. Referring to Figure 1 during the positive half-line cycle, the first DC–DC SEPIC circuit  $L_1$ – $Q_1$ – $C_1$ – $L_3$ – $D_o$  is active through diode  $D_p$ , which connects the input ac source to the output ground. During the negative half-line cycle, the second DC–DC SEPIC circuit,  $L_2$ – $Q_2$ – $C_2$ – $L_3$ – $D_o$ , is active through diode  $D_n$ , which connects the input ac source to the output ground. Thus, due to the symmetry of the circuit, it is sufficient to analyse the circuit during the positive half-period of the input voltage. The rectifier is operated when the switch  $Q_1$  is turned on then diode  $D_p$  is forward biased by the sum inductor currents  $i_{L1}$  and  $i_{L2}$ . As a result, diode  $D_n$  is reversed biased by the input voltage. The output diode is reversed biased by the reverse voltage ( $v_{ac} + V_o$ ). Thus, the loss due to the turn-on switching

losses and the reverse recovery of the output diode are considerably reduced., Equations for both rectifiers are identical, provided that the voltages on the capacitors for the SEPIC rectifier

$$V_{C1}(t) = V_{C2}(t) + V_{ac}(t) = \begin{cases} v_{ac}(t) & 0 \leq t \leq \frac{T}{2} \\ 0 & \frac{T}{2} \leq t \leq T \end{cases} \quad (1)$$

### 4 . MODES OF OPERATION

The circuit operation during one switching period  $T_s$  in a positive half-line period can be divided into three distinct operating modes, as shown in Fig 2 to Fig 4, and it can be described as follows.



**Fig 2 : Switch Q1 on topology**

*Mode 1* [ $t_0, t_1$ ],

In this stage, the three-inductor currents linearly increase at a rate proportional to the input voltage  $v_{ac}$ . The rate of increase of the three inductor currents is given by

$$\frac{di_{L_n}}{dt} = \frac{V_{ac}}{L_n} \quad n=1, 2, 3 \quad (2)$$

During this stage, the switch current is equal to the sum of the three inductor currents. Thus, the peak switch current  $I_{Q1-pk}$  is given by

$$I_{Q1pk} = \frac{V_m}{L_x} D_1 \quad (3)$$

where,

$$\frac{1}{L_x} = \frac{1}{L_1} + \frac{1}{L_2} + \frac{1}{L_3} \quad (4)$$

Let  $D_1$  be the duty cycle of switch  $Q_1$ . This interval ends when  $Q_1$  is turned off, initiating the next subinterval.

*Mode 2* [ $t_1, t_2$ ],

At the instant  $t_1$ , switch  $Q_1$  is turned off, diode  $D_o$  is turned on, simultaneously providing a path for the three inductor currents. Diode  $D_p$  remains conducting to provide a path for  $i_{L1}$  and  $i_{L2}$ . In this stage, the three inductor currents linearly decrease at a rate proportional to the output voltage  $V_o$ . The three inductors' currents are given by

Table 1 : Comparison Between Conventional And Bridgeless SEPIC PFC DCM Rectifier

Item		Bridgeless SEPIC	Conventional SEPIC
Slow diode		2	4
Fast diode		1	1
Switch		2	1
Current conduction path	Stage1	1 slow diode, 1 fast diode	2 slow diodes, 1 switch
	Stage2	1 slow diode, 1 fast diode	2 slow diodes, 1 fast diode
	DCM	1 slow diode	2 Slow diodes

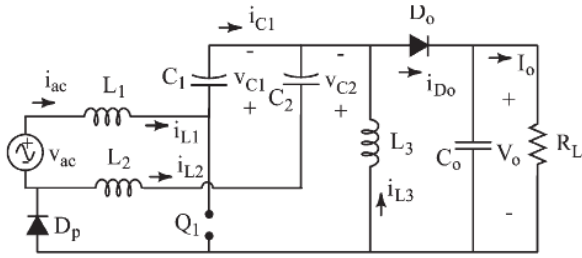


Fig 3 : Switch  $Q_1$  OFF topology

$$\frac{dL_n}{dt} = \frac{-V_n}{L_n} \quad n=1, 2, 3 \quad (5)$$

At the end of this mode the output diode current  $i_{Do}$  smoothly reaches to zero and  $Do$  becomes reverse biased. The normalized length of this interval is given by

$$D_2 = \frac{D_1}{M} \sin(\omega t) \quad (6)$$

Mode 3 [ $t_2, t_s$ ],

In this stage, both  $Q_1$  and  $Do$  are in their off-state. Diode  $D_p$  provides a path for  $i_{L3}$ . The three inductors behave as current sources, which keeps the currents constant. Hence by end of this interval, the voltage across the three inductors is zero. Capacitor  $C_1$  is charging up by  $i_{L1}$ , while  $C_2$  is discharged by  $i_{L2}$ .

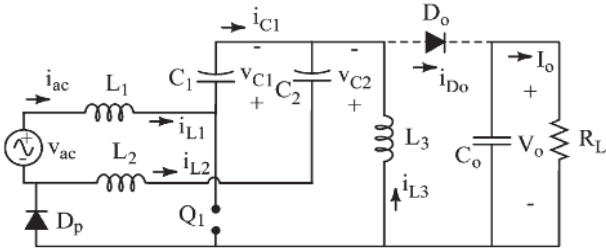


Fig 4 :DCM topology Solid and dashed lines represent active and inactive elements

## 5. COMPARISION BETWEEN CONVENTIONAL AND BRIDGELESS SEPIC PFC RECTIFIER

The circuit components in both the conventional PFC SEPIC rectifier and the improved bridgeless PFC SEPIC have similar peak voltage and current stresses. However, the bridgeless SEPIC is subjected to the input inductors ( $L_1$  and  $L_2$ ), the coupling capacitors ( $C_1$  and  $C_2$ ), and the active switches ( $Q_1$  and  $Q_2$ ) to a lower rms current stress compared to their counter parts in the conventional SEPIC topology. Moreover, the bridgeless SEPIC is constructed by connecting two DC-DC converters, each operating as SEPIC DC-DC converter, the switching performance of the two converters remains the same, which results in switching losses. Table 1 gives the comparison between conventional and bridgeless SEPIC PFC DCM based on the equipments and current conduction path

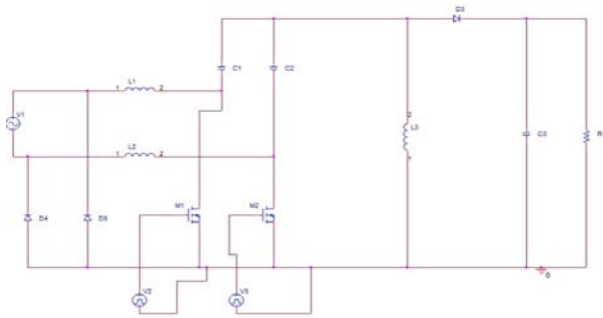
PSPICE actual semiconductor models have been used to simulate the semiconductor devices: STTH2003CR 300 V, 10 A,  $V_F = 0.85V$  high efficiency ultrafast diode for the output SEPIC diode and 1N5402 (200 V, 3 A,  $V_F = 1V$ ) standard recovery rectifier for the slow diodes. Three different MOSFETs (IRFB4332PBF with  $R_{DS-ON} = 29m\Omega$ , STY60NM50 with  $R_{DS-ON} = 45m\Omega$ , and IRF450 with  $R_{DS-ON} = 400m\Omega$ ), as well as an IGBT (HGTG40N60A4 with  $V_{CE-Sat} = 1.7V @ 40A$ ), actual models have been used for the active switches. Furthermore, for the bridgeless SEPIC PFC rectifier, a low voltage drop with very low reverse leakage current Schottky barrier diode (type PDS3200 with  $V_F = 0.63V @ 1A$ ) is connected in series with the power MOSFET to prevent any current from flowing through the MOSFET body diode.

## 6. SIMULATION RESULTS

The simulation results discussed by the Bridgeless DCM SEPIC PFC rectifier is shown in Fig 5 and then Bridgeless DCM SEPIC PFC rectifier with step change of +20V is shown in Fig 11 and at last the Closed loop pi control with Bridgeless DCM SEPIC PFC rectifier is given in Figure 15.

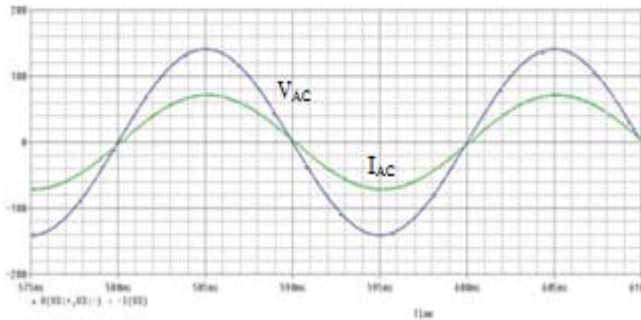
### 6.1. Simulation Model of Bridgeless DCM SEPIC PFC Rectifier

The simulation circuit of Bridgeless DCM SEPIC PFC rectifier is shown in Fig 5. The various waveforms obtained from the simulation are presented in Fig 6 to 10



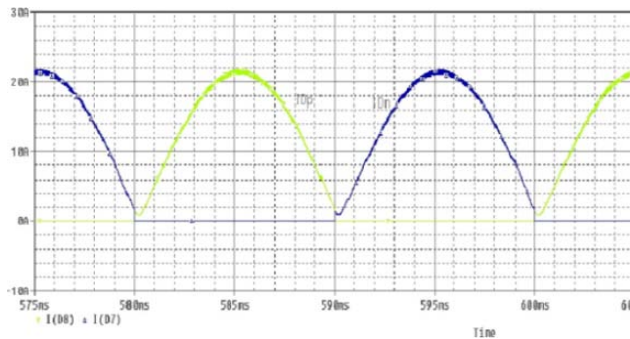
**Fig 5: Simulation circuit of Bridgeless DCM SEPIC PFC rectifier**

Fig 6 shows the waveform of  $V_{AC}$  and  $I_{AC}$ . From this waveforms, it is observed that the input line current is in phase with the input voltage .



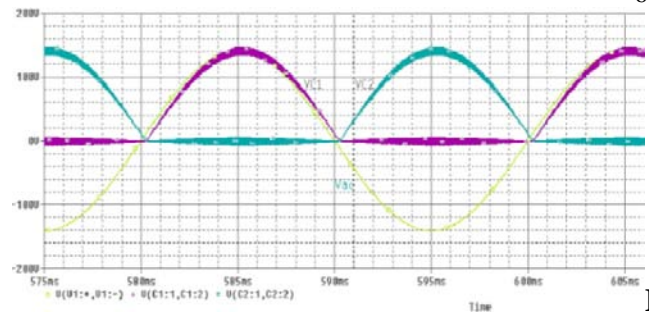
**Fig 6 :Waveforms of  $V_{AC}$  and  $I_{AC}$**

Fig 7 shows the two input diode currents namely positive diode current and negative diode current , conducting in alternate half-line cycles.



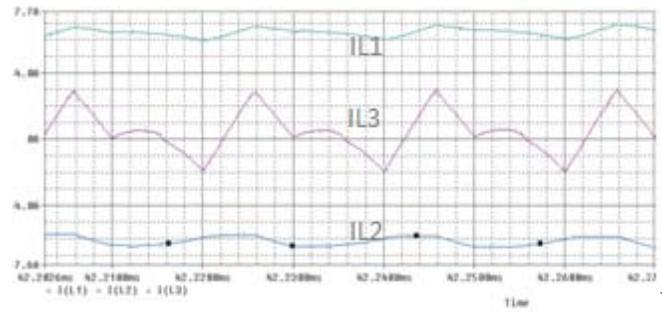
**Fig 7: Diode  $I_{Dp}$  and  $I_{Dn}$  current**

Voltage across the intermediate capacitor  $C_1, C_2$  along with the input voltage is shown in Figure 8.  $V_{C1}$  closely tracks the positive portion of the input AC voltage ( $V_{AC}$ ) and  $-V_{C2}$  closely tracks the negative portion of input AC voltage ( $V_{AC}$ ).



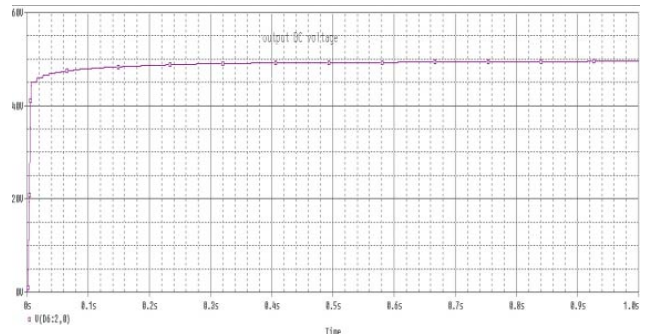
**g 8: waveforms for  $V_{AC}$ ,  $V_{C1}$  and  $V_{C2}$**

The inductor currents  $I_{L1}$  and  $I_{L2}$  and  $I_{L3}$  are shown in Fig 9. The three inductor currents at peak input voltage are depicted which correctly demonstrates the DCM operating mode.



**fig 9: Waveform  $I_{L1}$  and  $I_{L2}$  and  $I_{L3}$**

For an input rms voltage of 100V , it produces an output DC voltage of 48V ,the respective obtained results are displayed in Fig 10.



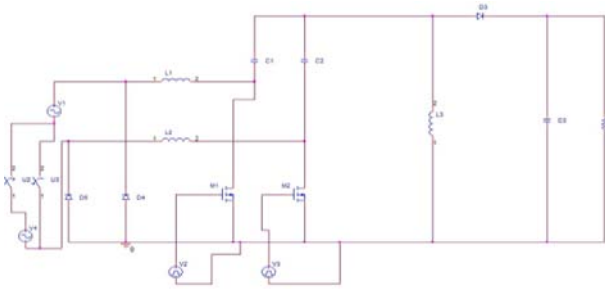
**Fig 10 : Output DC voltage waveform**

## 6.2. Simulation Model of Bridgeless DCM SEPIC PFC Rectifier with Step Input Change

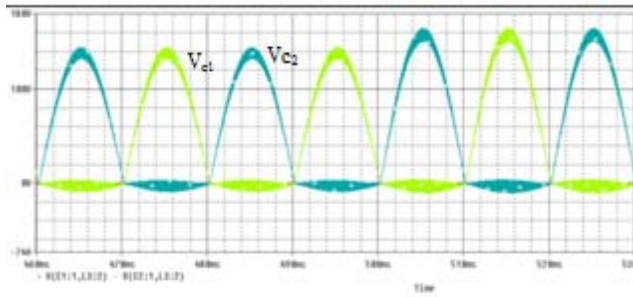
The simulation model of Bridgeless DCM SEPIC PFC rectifier with step change of +20V is shown in Figure 11. A voltage of +20V is added to the supply voltage of 100V to create a step change in the input. The circuit of Bridgeless DCM SEPIC PFC rectifier suffers a step input voltage change at 500ms and thereby it attains the steady state.

### 6.3 . Closed Loop PI Control with Bridgeless DCM SEPIC PFC Rectifier.

Fig 15 depicts the closed loop simulation circuit using PI controller, where input side voltage disturbances are created at a specified time.

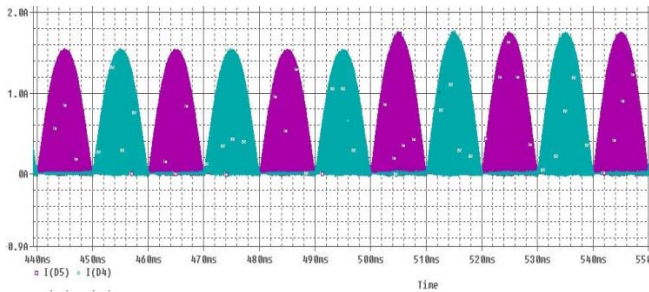


**Fig 11: Bridgeless DCM SEPIC PFC rectifier with input disturbance**

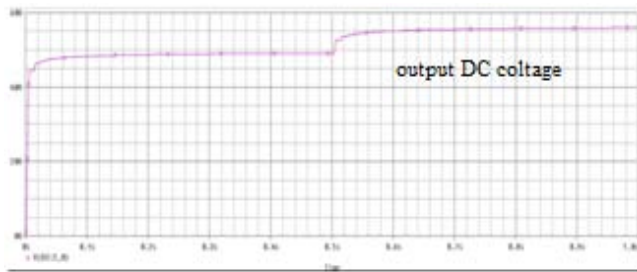


**Fig 12: Wwaveforms of  $V_{c1}$ ,  $V_{c2}$  during an step change**

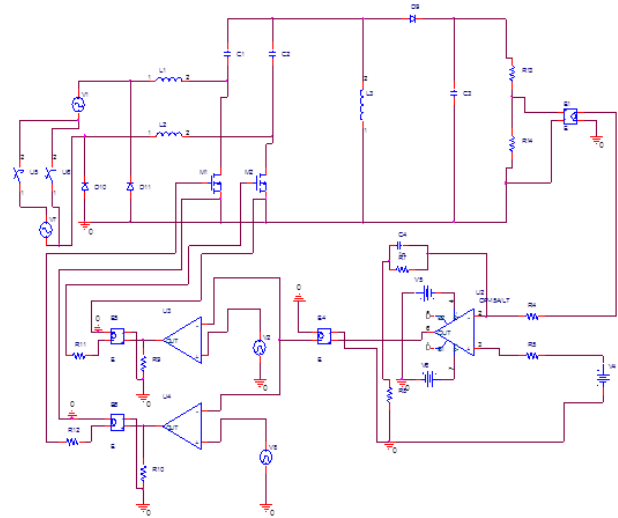
The magnitude of the voltage is 48 V till 500ms. From 500ms once there is input step change the voltage increase and reaches to 58V. The waveforms obtained for open loop with disturbance for  $V_{c1}$  and  $V_{c2}$  is shown in Figure 12. Open loop with disturbance waveforms for diode currents  $I_{Dp}$  and  $I_{Dn}$  are given in Figure 13 and output DC voltage is given in Fig 14.



**Fig 13: Open loop with disturbance waveforms for Diode  $I_{Dp}$  and  $I_{Dn}$  current**

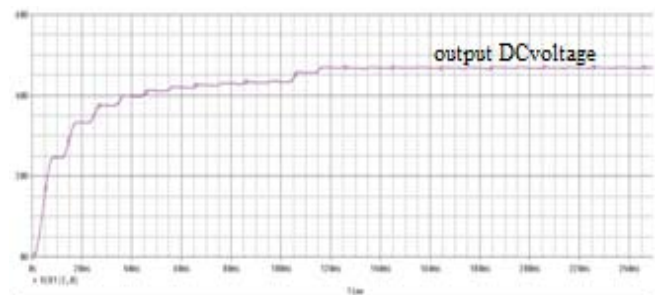


**Fig 14: Output DC voltage waveform with open loop with disturbance**



**Fig 15: Closed Loop PI Control Bridgeless DCM SEPIC PFC Rectifier**

The output voltage of open loop with disturbance remains constant till the time of disturbance given by PI controller. The input voltage disturbance given using PI controller gets reflected in the output side, leading to reduction in the output voltage. The closed loop PI circuit with PWM controller helps in reducing the overshoot caused due to open loop with disturbance. The output voltage is continuously compared with a reference voltage using a differential amplifier. The differential signal is amplified and fed to a comparator, which compares it with a triangular wave. The comparator output is fed to one of the MOSFET switches. Another triangular wave is phase shifted by  $180^\circ$  is compared with the same differential amplifier output and the output of the second comparator is fed to the other MOSFET. Thus changes in the output voltage are reflected in the differential amplifier output and in turn in the comparator output. Figure 16 gives the output DC voltage of the closed loop circuit.



**Fig 16 :Closed Loop DC output voltage**

## 7 . CONCLUSION

The single-phase bridgeless rectifiers with low input current distortion and low conduction losses have been presented and analysed. The bridgeless rectifier is derived from the conventional SEPIC converter. Comparing with conventional SEPIC and Power Factor Correction circuits, due to the lower conduction loss and switching loss, Bridgeless DCM SEPIC PFC rectifier topologies can further improve the conversion efficiency. To maintain same efficiency, the improved circuits could operate with higher switching frequency. Thus, additional reduction in the size of PFC inductor and EMI filter could be achieved. Besides improving circuit topology and performance, a further reduction in rectifier size could be realized by integrating the three inductors into a single magnetic core.

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